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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,905	09/28/2001	J.G. Walacavage	200-0664	4248
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			<div>EXAMINER PROCTOR, JASON SCOTT</div>	
			<div>ART UNIT 2123</div>	<div>PAPER NUMBER</div>
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/965,905

Applicant(s)

WALACAVAGE ET AL.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8,10 and 12-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8,10 and 12-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/7, 3/16/2007</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-8, 10, and 12-21 were rejected in the Office Action of 4 December 2006.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 February 2007 has been entered.

The 8 February 2007 submission has amended claims 1, 12, and 21. Claims 1-8, 10, and 12-21 are pending in this application.

Claims 1-8, 10, and 12-21 are rejected.

1. Applicants argue primarily that:

LeBaron et al. does not disclose playing a simulation model by a PLC logical verification system on a computer...

The Examiner traverses this argument as follows.

LeBaron expressly teaches "*Routing logic, PLC or PC control software, sequencing algorithms, and more can be integrated, tested, and debugged within a simulation environment.*" (abstract, emphasis added). "*Emulation of the Rapistan control system for this project integrates a simulation model with the actual control system. The simulation model provides the output for evaluating control logic and algorithms.*" (page 1055, right column, emphasis added). See also Figure 2, which plainly shows "Routing Logic, Scheduling

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Algorithms, Host Controllers, and **PLC/PC Testing**” interacting with “**Simulation Model: Graphical Animation**, Statistical Output.” (page 1056, Figure 2, emphasis added)

2. Applicants further argue that:

LeBaron et al. does not disclose ... allowing a user to visually see flow of a part through the manufacturing line, wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line...

The Examiner respectfully traverses this argument as follows.

Applicants’ claim language requires that the reference allows this feature in order to be anticipatory. This language is interpreted as similar to “does not prevent”. The LeBaron reference “does not prevent” a use from visually seeing flow of a part through the manufacturing line, etc., nor do Applicants contend that it does.

Further, the LeBaron reference expressly teaches that “*the simulation model also provides real time 3-D graphical animation for improved visibility and confidence.*” (page 1055, right column).

3. Applicants further argue that:

LeBaron et al. does not disclose ... generating the PLC code if a part flow represented in the simulation model is correct.

The Examiner respectfully traverses this argument as follows.

The LeBaron reference expressly teaches that “*by developing and refining the control logic and algorithms in the control software, it exists as developed.*” (page 1055, right column).

That is, **the code developed in the control software** is one and the same with **PLC code to be used in the actual equipment**.

4. Applicants further argue that:

LeBaron et al. also does not disclose using the generated PLC code and implementing the manufacturing line according to the part flow simulation model.

The Examiner respectfully traverses this argument as follows.

LeBaron expressly teaches *"Because the actual control system is used to develop, test, and refine algorithms and logic, it exists as developed in the real system."* (page 1055, left column). A person of ordinary skill in the relevant art would understand this to mean that the purpose of emulation in the LeBaron reference is to test algorithms and logic for the express purpose of implementation in a manufacturing line.

5. Applicants further argue that:

In LeBaron et al., there is no PLC logical verification system and no PLC code is generated.

The Examiner respectfully traverses this argument as follows.

LeBaron expressly teaches *"Routing logic, PLC or PC control software, sequencing algorithms, and more can be integrated, tested, and debugged within a simulation environment."* (abstract, emphasis added) *"Because the actual control system is used to develop, test, and refine algorithms and logic, it exists as developed in the real system."* (abstract, emphasis added).

6. Applicants further argue that:

The PLC logical verification system is not a software representation of a physical device, but a software tool that allows dynamic interaction directly with a simulation model to test PLC logic by having an input and output exchange similar to input-output control logic to validate that the logic is delivering what is intended.

The Examiner respectfully traverses this argument as follows.

Applicants' argument appears contradictory. A PLC is a well-known physical device that performs, among other functions, input-output processing according to control logic. Applicants' argument appears to say that the PLC logical verification system is not a software representation of a physical device, but a software tool [i.e., a software representation] ... having an input and output exchange similar to input-output control logic [i.e. replicating the behavior of a physical device such as a PLC].

7. Applicants further argue that:

In LeBaron, et al., the emulator does not validate that the logic is delivering what is intended.

The Examiner respectfully traverses this argument as follows.

In Applicants' claim language, the programmable logic verification system does not validate that the logic is delivering what is intended.

The language of independent claims 1, 12, and 21 generically recite "methods" comprising, *inter alia*, a step of "determining if the part flow represented in the simulation model is correct." None of these claims recite that the programmable logic verification system performs this step.

8. Applicants further argue that:

LeBaron et al. also lacks using the generated PLC code and implementing the manufacturing line according to the part flow simulation model. In LeBaron et al., while LeBaron et al. mentions PLC or PC control software can be tested and debugged within a simulation environment, there is no part flow for a programmable logic controller logical verification system and there is no generated PLC code that is used in implemented a manufacturing line.

The Examiner respectfully traverses this argument as follows.

The arguments regarding generation of PLC code have been addressed above.

LeBaron expressly teaches "*The material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations... A graphical representation of the pick and pack conveyor system is shown in Figure 1.*" (page 1055, left column, emphasis added). Figure 1, "**flow**".

Applicants' argument have been fully considered but have been found unpersuasive.

Upon further consideration of the reference, the Examiner withdraws the 35 U.S.C. § 102 rejection and instead applies a 35 U.S.C. § 103 rejection to reflect that the claims are unpatentable over the teachings of the reference as viewed by a person of ordinary skill in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

1. Claims 1-8, 10, and 12-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over “Emulation of a Material Delivery System” by Todd LeBaron and Kelly Thompson (LeBaron).

Regarding claims 1, 12, 20, and 21, LeBaron teaches:

A computer-implemented method for verification of part flow in a system [*“Emulation of the complex pick and pack conveyor system will be presented.”* (page 1055, left column, Abstract); *“The material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations.”* (page 1055, left column, System Description)] including a programmable logic controller verification [*“Routing logic, PLC or PC control software, sequencing algorithms, and more can be integrated, tested, and debugged within a simulation environment.”* (Henceforth “control logic” refers to at least controller logic in a PLC.) (page 1055, left column, Abstract); *Emulation has been used for a*

Rapistan Systems project to test, debug, and optimize complex algorithms and control logic." (page 1055, left column, Abstract)], comprising the steps of:

Constructing a simulation model of a part flow in a manufacturing line using a computer [*"The material handling system consists of conveyor sections which continuously move carriers around a closed loop that connects all pick and pack stations."* (A part flow in a manufacturing line.) (page 1055, left column, System Description); *"Emulation of the complex pick and pack conveyor system will be presented."* (page 1055, left column, Abstract)];

Representing a part and part locations of the manufacturing line [*"A graphical representation of the pick and pack conveyor system is shown in Figure 1."* (page 1055, left column, System Description); (Figure 1, page 1056)];

Playing the simulation model by a PLC logical verification system on the computer [*"Emulation of the Rapistan control system for this project integrates a simulation model with the actual control system. The simulation model provides the output for evaluating control logic and algorithms."* (page 1055, right column, Emulation); *"The simulation model provides the output for evaluating control logic and algorithms. The simulation model also provides real time 3-D graphical animation for improved visibility and confidence."* (page 1055, right column, Emulation)];

And allowing a user to visually see flow of a part through the manufacturing line, [LeBaron does not disclose *prohibiting* a user from visually seeing flow of a part through the manufacturing line and therefore anticipates this claim language. Further, LeBaron discloses a "Simulation Model: Graphical Animation" (page 1056, Figure 2) and *"The simulation model*

also provides real time 3-D graphical animation for improved visibility and confidence.” (page 1055, right column, Emulation)],

Wherein the PLC logical verification system dynamically interacts through input and output with the simulation model to verify a PLC code of the manufacturing line [*“The simulation model has a built-in message handler that receives and sends messages through a standard network interface (TCP/IP)... In addition, the simulation model sends messages to the server when certain events have occurred within the simulation model. This process is illustrated in Figure 2.” (page 1055, right column); Figure 2 (page 1056)];*

Determining if the part flow represented in the simulation model is correct [*“The emulation used at Rapistan Systems was able to prove that the system could handle the projected growth in daily orders.” (page 1060, left column, Summary)];*

Modifying the part flow represented in the simulation model if the part flow represented in the simulation model is not correct [*“RULE1 was developed to improve the FIFO algorithm.”, (page 1058, right column, The RULE1 Algorithm)]; and*

Using the part flow simulation model to test PLC code [*“Emulation provides the graphical and statistical output needed to accurately evaluate different algorithms and control logic.” (page 1060, left column, Summary)] and implementing the manufacturing line according to the part flow simulation model [*“Because the actual control system is used to develop, test, and refine algorithms and logic, it exists as developed in the real system. This eliminates re-implementation errors and provides greater confidence in the emulation results. (page 1055, left column, Abstract); “during the refinement process, two initial algorithms were developed and compared. These two algorithms are called the FIFO and RULE1.” (page 1057, right column,**

Algorithm Development); *"The emulation results indicate that using the correct order scheduling and pack assignment algorithm is key to improving pack station utilization and system throughput."* (page 1060, left column, Analysis)].

Although the language of LeBaron may differ slightly from the explicit language of the claim, each of the claimed elements are present in the teachings of LeBaron. Further, a person of ordinary skill in the art at the time of Applicants' invention would find it obvious to make certain connections based upon the teachings of LeBaron, motivated by common sense and his own knowledge of the background, such as recognizing that the abstract of LeBaron, in combination with the rest of the reference, teaches a system for developing "PLC or PC control software" for implementation in real "material handling systems." For this reason, LeBaron renders obvious the invention specified in claims 1-8, 10, and 12-21.

Regarding claims 2-5 and 13-16, LeBaron teaches selecting a part generator, generating a part with the part generator, and identifying part locations of the generated part within the manufacturing line [*"Emulation of the complex pick and pack conveyor system will be presented."* (page 1055, left column, Abstract); *"All of the components for a particular order are assigned and routed to a specific pack station."* (page 1055, right column, System Description); The analysis is conducted for a simulated 23-hour period (page 1060, left column, Analysis) which implicitly discloses the generation of components for a particular order so that the emulation can fulfill the order.].

Regarding "testing the generated part at the part location", the specification teaches this limitation as determining if the part is present or not present (specification as amended, page 12,

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lines 9-11). LeBaron discloses emulation of a pick and pack conveyor system and therefore implicitly discloses “testing the generated part at the part location” as the ability to detect if the part is present or not present is a basic underlying principle in the proper operation of a pick and pack conveyor system. Further emphasis of this is LeBaron’s disclosure [*“The goal in developing algorithms was to process the required number of orders per day within the planned facility schedule. Fully utilizing the pack stations is key in accomplishing this goal.”* (page 1057, right column, Problem Description)] that clearly implies that pack stations can determine whether a necessary generated part is present at that pack station.

Regarding claims 6-8 and 17-19, LeBaron teaches constructing records for the parts [orders] wherein the record has at least one resource and at least one capability [*“Historical data was used to generate daily order profiles (as in Table 1).”* (page 1057, right column, Problem Description); Table 1 shows records [orders] for the parts, including a resource [Pick Station] and a capability [# Pick Types]].

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

“A Simulation-Based Controller Builder for Flexible Manufacturing Systems” by Fernando Gonzalez describes a simulation environment including a simulation model which can control a physical emulator of a flexible manufacturing system (abstract).

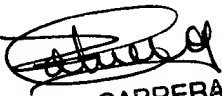
"A Simulation-Based Controller for Distributed Discrete-Event Systems with Application to Flexible Manufacturing" by Fernando Gonzalez and Wayne Davis expands upon the reference noted above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123


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